

Remarks/Arguments

Claims 1-9 are pending in the present application. Claims 1-5 and 7-9 have been amended.

Drawings

Applicant notes the Examiner's acceptance of the formal drawings as filed along with the present application on February 28, 2002.

Claim Rejections-35 U.S.C. 102

Claims 1-9 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Eguchi reference (U.S. Patent No. 5,444,186), or in the alternative by the Keri reference (U.S. Patent No. 5,861,656). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 1 includes in combination a circuit area; a metal guard ring "having an inside edge, an outside edge, and a slit disposed between the inside edge and the outside edge"; and a passivation layer "having a slot disposed above the metal guard ring, the slot extending down to the metal guard ring and surrounding the circuit area, the slot being located away from the slit, so that the slit is covered by the passivation layer". Applicant respectfully submits that the prior art as respectively relied upon by the Examiner in the alternative does not disclose these features.

With regard to the Eguchi reference, the Examiner has interpreted elements 18 and 17 in Figs. 18A and 18B as the metal guard ring of claim 1. However, as described in column 3, lines 35-49 of the Eguchi reference, an aluminum wire 16, a bonding pad 17 and a guard ring 18 are provided on the surface of second surface insulating film 15.

Bonding pad 17 is not a guard ring as asserted by the Examiner. Accordingly, the opening in passivation film 21 as particularly illustrated in Fig. 18B of the Eguchi reference is above bonding pad 17, not above guard ring 18, and the opening does not extend down to guard ring 18, as would be necessary to meet the features of claim 1.

Applicant therefore respectfully submits that the semiconductor device of claim 1 distinguishes over the Eguchi reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-4, is improper for at least these reasons.

Applicant also respectfully submits that the method of manufacturing a semiconductor device of claim 5 distinguishes over the Eguchi reference as relied upon by the Examiner for at least somewhat similar reasons as set forth above. Particularly, the Eguchi reference as relied upon by the Examiner does not disclose a method including in combination forming a slot in a passivation layer above a metal guard ring, so that the slot extends down to the metal guard ring, as would be necessary to meet the features of claim 5. Accordingly, Applicant respectfully submits that the method of manufacturing a semiconductor device of claim 5 distinguishes over the Eguchi reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 5-9, is improper for at least these reasons.

Regarding the Keri reference, the Examiner has apparently interpreted metal conductor 30 in Figs. 5 and 6 as the metal guard ring of the claims, whereby a slot is formed in passivation 18 above the metal conductor 30. However, metal conductor 30 as particularly illustrated in Fig. 6, does not include “an inside edge, an outside edge, and a slit disposed between the inside edge and the outside edge”, as would be necessary to meet the features of claim 1. That is, there is no slit in conductor 30. Consequently, the Keri reference does not disclose a slot extending down to a metal guard ring and surrounding a circuit area, with “the slot being located away from the slit, so that the slit

is covered by the passivation layer”. Accordingly, Applicant respectfully submits that the semiconductor device of claim 1 distinguishes over the Keri reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-4, is improper for at least these reasons.

Also, since the Keri reference as relied upon by the Examiner does not include a slit, the Keri reference clearly does not disclose the features of claims 3 and 4 that are further directed to the slit. Applicant therefore respectfully submits that claims 3 and 4 distinguish over the Keri reference as relied upon by the Examiner for at least these additional reasons.

Applicant also respectfully submits that the method of manufacturing a semiconductor device of claim 5 distinguishes over the Keri reference as relied upon by the Examiner. Particularly, the Keri reference does not disclose forming a metal guard ring “having an inside edge, an outside edge, and a slit disposed between the inside edge and the outside edge”, as would be necessary to meet the features of claim 5. Also, since the Keri reference as relied upon by the Examiner does not disclose a slit, the Keri reference clearly fails to disclose the features of claims 8 and 9 that are further directed to the slit. Applicant therefore respectfully submits that the method of manufacturing a semiconductor device of claim 5 distinguishes over the Keri reference, and that this rejection, insofar as it may pertain to claims 5-9, is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present

application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

A handwritten signature in black ink, appearing to read "A. J. Telesz, Jr.", followed by a large checkmark.

Andrew J. Telesz, Jr.
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